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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/808,056	03/24/2004	Enver Krvavac	MOTB:035US	4214

7590 06/24/2005

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EXAMINER	
CHOE, HENRY	

ART UNIT	PAPER NUMBER
2817	

DATE MAILED: 06/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/808,056	KRVAVAC ET AL.	
	Examiner	Art Unit	
	Henry K. Choe	2817	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/24/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-24 are rejected under 35 U.S.C. 102(e) as being anticipated by Thompson (Figs. 2-4).

Regarding claims 1, 5-7, 11, 12, 14-17, 19 and 21-23, Thompson (Figs. 2-4) discloses an amplifier circuit comprising a semiconductor die (a largest rectangle box in Fig. 2), a Doherty amplifier (102 in Fig. 2) integrated on the semiconductor die (see column 5, lines 17-22), the Doherty amplifier (102 in Fig. 2) including a peaking amplifier (112 in Fig. 2) and a carrier amplifier (110 in Fig. 2) which is coupled to the peaking amplifier (112 in Fig. 2), a bias circuit (104 in Fig. 2) which is integrated on the semiconductor die and coupled to the Doherty amplifier (102 in Fig. 2), and a voltage offset circuit (VX404 in Fig. 4) which is integrated on the semiconductor die and coupled to the bias circuit (104 in Fig. 2) and to the Doherty amplifier (102 in Fig. 2) and the voltage offset circuit (VX404 in Fig. 4) and the bias circuit (104 in Fig. 2) together biasing the Doherty amplifier (102 in Fig. 2).

Regarding claims 2, 8 and 18, the bias circuit (104 in Fig. 2) including a FET (246).

Regarding claims 3, 9, 10 and 20, the voltage offset circuit (VX404 in Fig. 4) which determines a drive level at which the peaking amplifier (112 in Fig. 2) is turned to an ON mode since the voltage offset circuit is connected to the base of the peaking amplifier transistor and wherein the voltage offset circuit (VX404 in Fig. 4) is a fixed voltage.

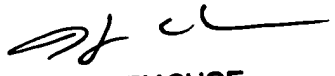
Regarding claims 4, 13 and 24, a resistor divider network (238 in Fig. 3) integrated on the semiconductor die (a largest rectangle box in Fig. 2) and coupled to the carrier amplifier (110 in Fig. 2) and the resistor divider network (238 in Fig. 3) biasing the peaking amplifier (112 in Fig. 2).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Patent numbers (6,262,629; 5,757,229; 4,074,181) are the Doherty amplifiers.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Henry Choe whose telephone number is (571) 272-1760.



HENRY CHOE
PRIMARY EXAMINER

#1028